CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A system having a motherboard, the motherboard comprising:
a first set of connections facilitating a first port to support a symmetric PCI Express data transfer when in a first mode of operation; and
a second set of connections facilitating a second port to support an asymmetric PCI Express data transfer when in a second mode of operation, wherein the second set of connections is a subset of the first set of connections.

2. (Previously Presented) The system of claim 1 wherein the first set of connections includes a plurality of bidirectional lane pairs and the second set of connections includes at least one unidirectional lane pair to support a unidirectional data transfer when in the second mode of operation.

3. (Original) The system of claim 1 further comprising:
a mode detect module to determine a mode of operation as one of the first mode of operation and the second mode of operation.

4. (Original) The system of claim 1 further comprising the system being a host interface controller.

5. (Original) The system of claim 4, wherein the host interface controller is associated with a north-bridge controller.

6. (Original) The system of claim 1 further comprising the system being an image controller.

7. (Original) The system of claim 6 wherein the image controller is a graphics controller.

8. (Original) The system of claim 6 wherein the image controller is a video controller.

9. (Original) The method of claim 1, wherein during the second mode of operation a number of data transmit connections is greater that a number of data receive connections.

10. (Original) The method of claim 1, wherein during the second mode of operation a number of data receive connections is greater that a number of data transmit connections.

11. (Original) The method of claim 1, wherein during the second mode of operation a number of data receive connections is greater that a number of data receive connections.

12. (Original) The method of claim 4, wherein during the second mode of operation a number of data receive connections is greater that a number of data transmit connections.

13. (Currently Amended) A method comprising:

when in a first mode of operation:

transmitting data to a first peripheral system over a first plurality of PCI Express port connectors; and

receiving data from the first peripheral system over a second plurality of PCI Express port connectors, wherein the second plurality is less than the first plurality;

transmitting data to a second peripheral system over a third plurality of PCI Express port connections; and

receiving data from the second peripheral device over a fourth plurality of PCI Express port connections, wherein the fourth plurality is equal in quantity to the third plurality.

14. (Cancelled)

15. (Currently Amended) The method of claim [[14]]13 further comprising:

when in a second mode of operation

transmitting data to a third peripheral system over the first plurality of PCI Express port connections; and

receiving data from the third peripheral device over the second, third and fourth plurality of PCI Express port connections.

16. (Original) The method of claim 13 further comprising:

determining a mode of operation to be one of a first mode of operation and a second mode of operation; and

configuring a system to operate in the mode of operation.

17. (Previously Presented) A system comprising a PCI Express port comprising a plurality of single bit transmitter/receiver pairs having one or more control inputs to configure the transmitter/receiver pair as a transmitter when the one or more control inputs receives a first select value, and as a receiver when the select input receives a second select value.

18. (Original) The system of claim 17 wherein one of the one or more control inputs is to hold the transmitter in a high impedance state.

19. (Original) The system of claim 17 wherein the plurality comprises a number of four or greater.

20. - 32. (Canceled)